UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,937,246 B2
DATED : August 30, 2005
INVENTOR(S) : Aaftab Munshi and James R. Peterson

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

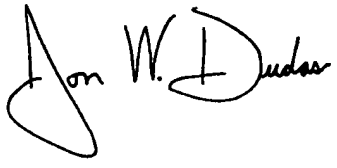
Column 3,
Line 31, reads, "the expansion bus 0.24 and memory/bus interface 20."; should read -- the expansion bus 24 and memory/bus interface 20. --.

Column 6,
Line 65, reads, "In an alternative embodiment, a unique ID number may"; should read -- In an alternative embodiment, a unique ID number may be --.

Column 7,
Line 28, reads "with respect to large caches, however, it will appreciated that"; should read -- with respect to large caches, however, it will be appreciated that --.

Signed and Sealed this

Third Day of January, 2006



JON W. DUDAS
Director of the United States Patent and Trademark Office